REMARKS

Claims 1-7 are pending in the application. Claims 1-7 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ishihara et al. (Ishihara).

Claim 8 is newly added. This claim is supported by the original specification, for example Fig. 2. No new matter is entered.

Applicant's claimed cross-connection switch stores time-division multiplex signals inputted from a plurality of lines into memory, and switches the signals for each time slot by assigning data to be outputted to each line based on the stored data's address and then reading and outputting the data.

With regard to claim 1 the Office Action points to Ishihara, table 27 and buffer 25 to show the first and second memory. The prior art teaches in col. 9: lines 55-57 that the write address controller 27 refers to the address management table 27 to generate the write addresses.

This is different from applicant's claimed invention which recites: counting a number of input time slots of an input frame, and outputting the count value as a read address and a write address respectively to said first memory and said second memory.

In applicant's claimed invention the counter provides the write address to the second memory whereas in the prior are the write address is generated from the address management table 27.

As shown in Fig. 2 of the present specification, the present invention comprises a memory 1 writing input data (second memory), a memory 2 (first memory) performing the address control of the memory 1 (time slot control), a counter 3 regularly supplying addresses to the memory 1 and memory 2 using a clock in order to synchronize the address with input data.

Comparing Fig. 2 to the examples in Figs. 6, 9 and 12, respectively, the memory 1 corresponds to the memory 11/21/31, the memory 2 to memory 12/22/32 and the counter corresponds to counter 13/23&24/33&34.

With regard to claim 2

Ishihara inserts a header in data corresponding to a payload when assembling ATM cells. Basically Ishihara stores the data and reads it by designating an address. In Ishihara, col. 9 time-division multiplexing as applying time-division multiplexing in units of cells is disclosed.

However Applicant's claim 2 provides when a multiplexed line signal having an input frame of n bits per channel is processed, a time slot number of each bit of an n-bit channel is assigned to addresses of said first memory means, and data indicating switching information about a time slot of each piece of bit data is entered at each address of said second memory means.

In the present invention, the memory 1 can control time slot position in units of bits, according to time slot information written in the memory 2. This feature is neither suggested nor disclosed by Ishihara.

Ishihara comprises a means for storing voice packets inputted to input lines #1 through #3 in a memory buffer 25 and reading the packets from the memory buffer in timing faster than that of inputted voice packet, and multiplexes short cells with voice packets by switching signals from a short cell header generator part and the output of a buffer memory, by a selector 26.

A multiplexing part 28 switches signals from an ATM cell header generator part and signals from short assembly parts 21_1 through 21_3 by a selector 30 by adjusting the output timings of the short assembly parts 21_1 through 21_3. Then, by switching the signals from the ATM cell header generator part and signals from the short assembly parts 21_1 through 21_3 by the

selector 30, the multiplexing part 28 multiplexes ATM cell headers with the signals, and outputs the multiplexed signals to an output line as ATM cells. In this case, short cells or an existing AAL format is generated under the control of a controller 27, basically using an existing circuit for the short assembly parts 21_1 through 21_3.

Applicant's claim 5 further comprises the 8-1 selector 14/non/36, FF non/25/37, selector non/26/38, phase adjustment unit non/27/36 of Figs. 6, 9 and 12, respectively.

In Figs. 6 and 12, time slot position control in units of bits can be realized among a plurality of lines by using the 8-1 selector.

Applicant's claim 5 further comprises flipflop means for holding data of a time slot read from said second memory means. In Figs. 9 and 12, the FF, selector and phase adjustment unit are provided in order to set the delay of an input signal as close to 0 as possible.

It is respectfully submitted the present invention is not anticipated by Ishihara because neither time slot operation for each bit nor time slot position control for each voice packet is performed and voice packets inputted to the short assembly parts 21_1 through 21_3 constitute the process unit taught by Ishihara.

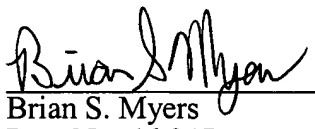
The delay of an input signal is not also taken into consideration. Therefore, an output signal greatly lags behind the input signal.

For at least the foregoing reasons it is respectfully requested the rejection be withdrawn and claims 1-8 be placed in condition for allowance.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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